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10872 U.S. PRO
09/76953

		Subclass
	Class	ISSUE CLASSIFICATION

PATIENT NUMBER

Best Available Copy

U.S. UTILITY Patent Application

KW	O.I.P.E.	PATENT DATE
SCANNED	28(3) Q.A.	LA

APPLICATION NO. 09/769953	CONT/PRIOR	CLASS 706	SUBCLASS 714	ART UNIT 2122 -32114	EXAMINER R. carroll
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Sompong Olarig

TIME

Computer system having configurable core logic chipset for connection to a fault-tolerant accelerated graphics port bus and peripheral component interconnect bus

PTO-2040
13/98

ISSUING CLASSIFICATION

<input checked="" type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
<input checked="" type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent No. <u>6,018,810</u>				ISSUE FEE	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.				ISSUE BATCH NUMBER	

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